

09610788 070600

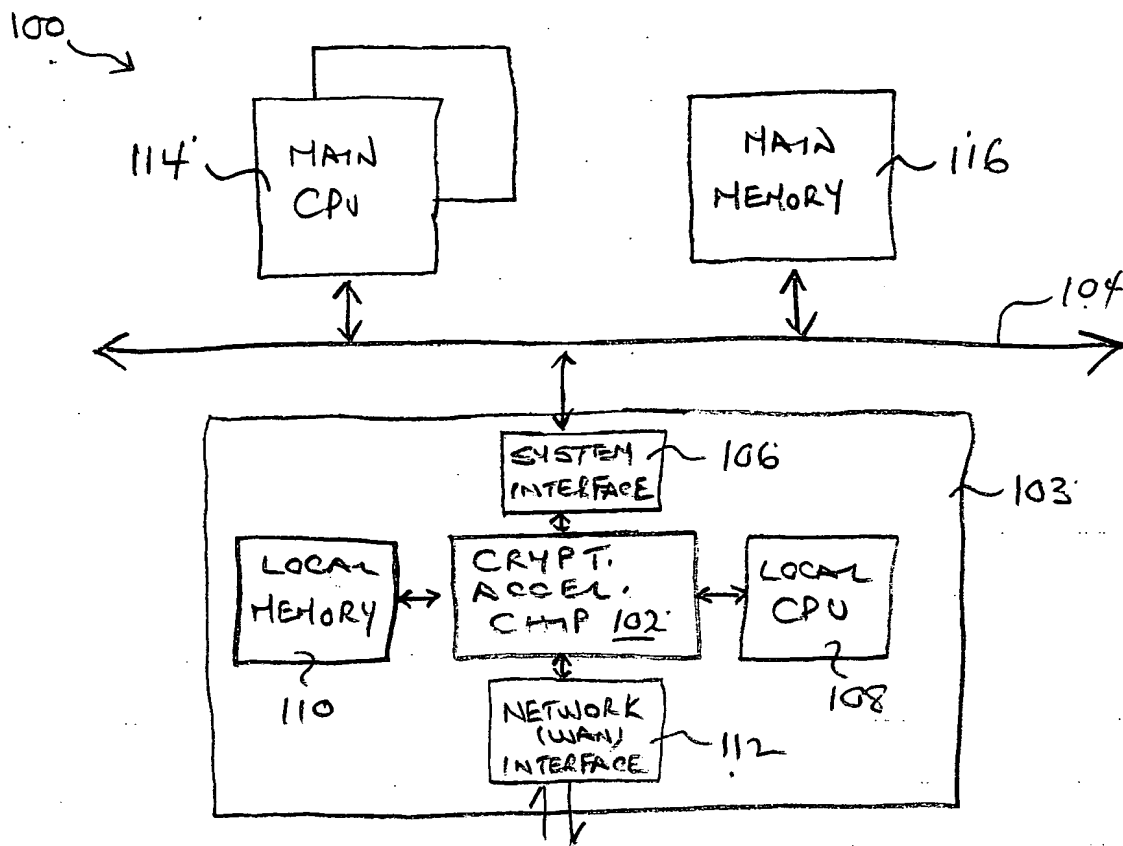


FIG. 1A

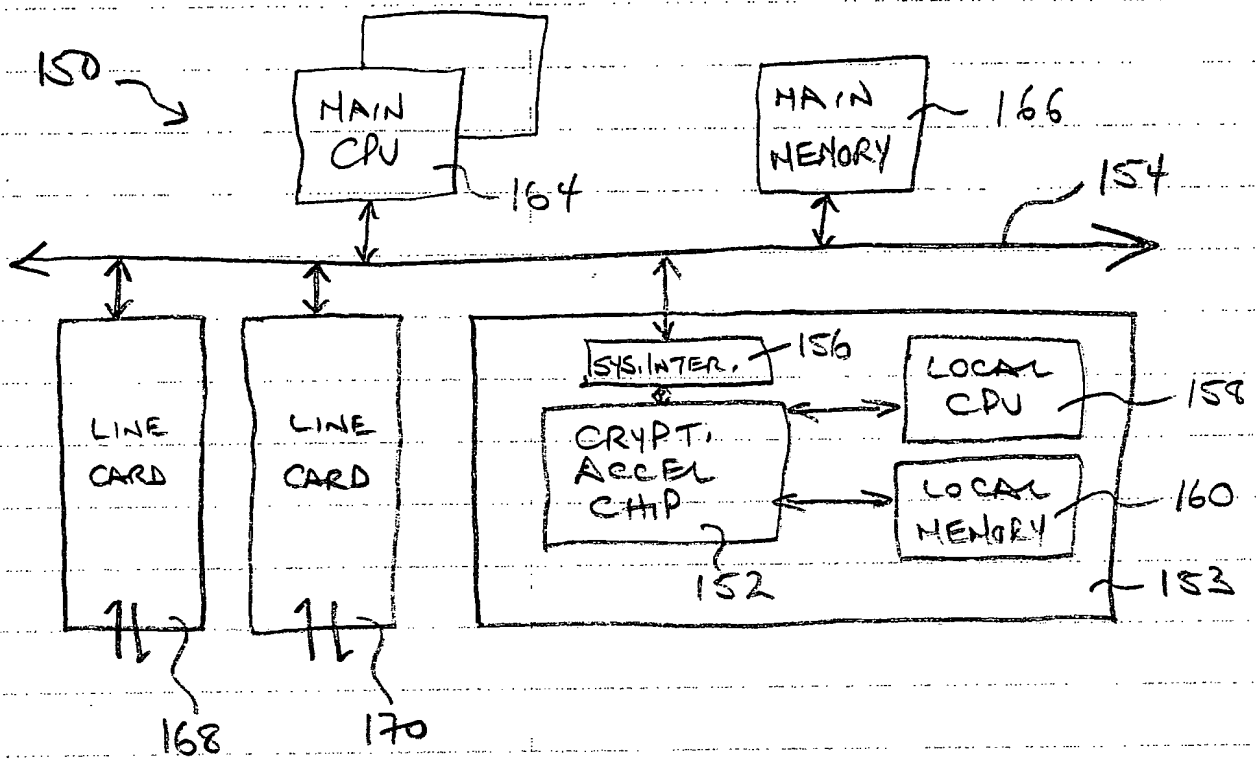


FIG. 1B

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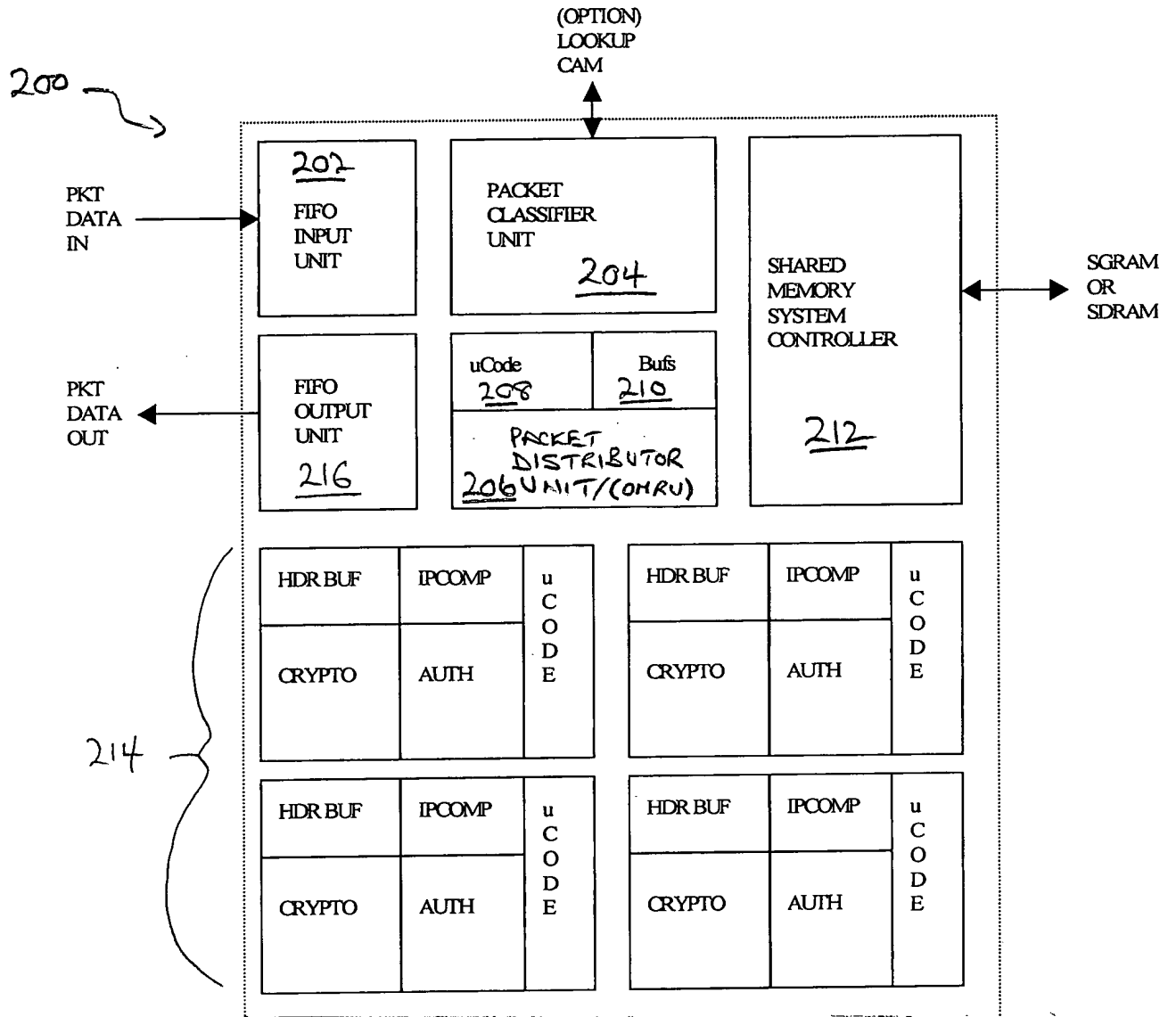


FIG. 2

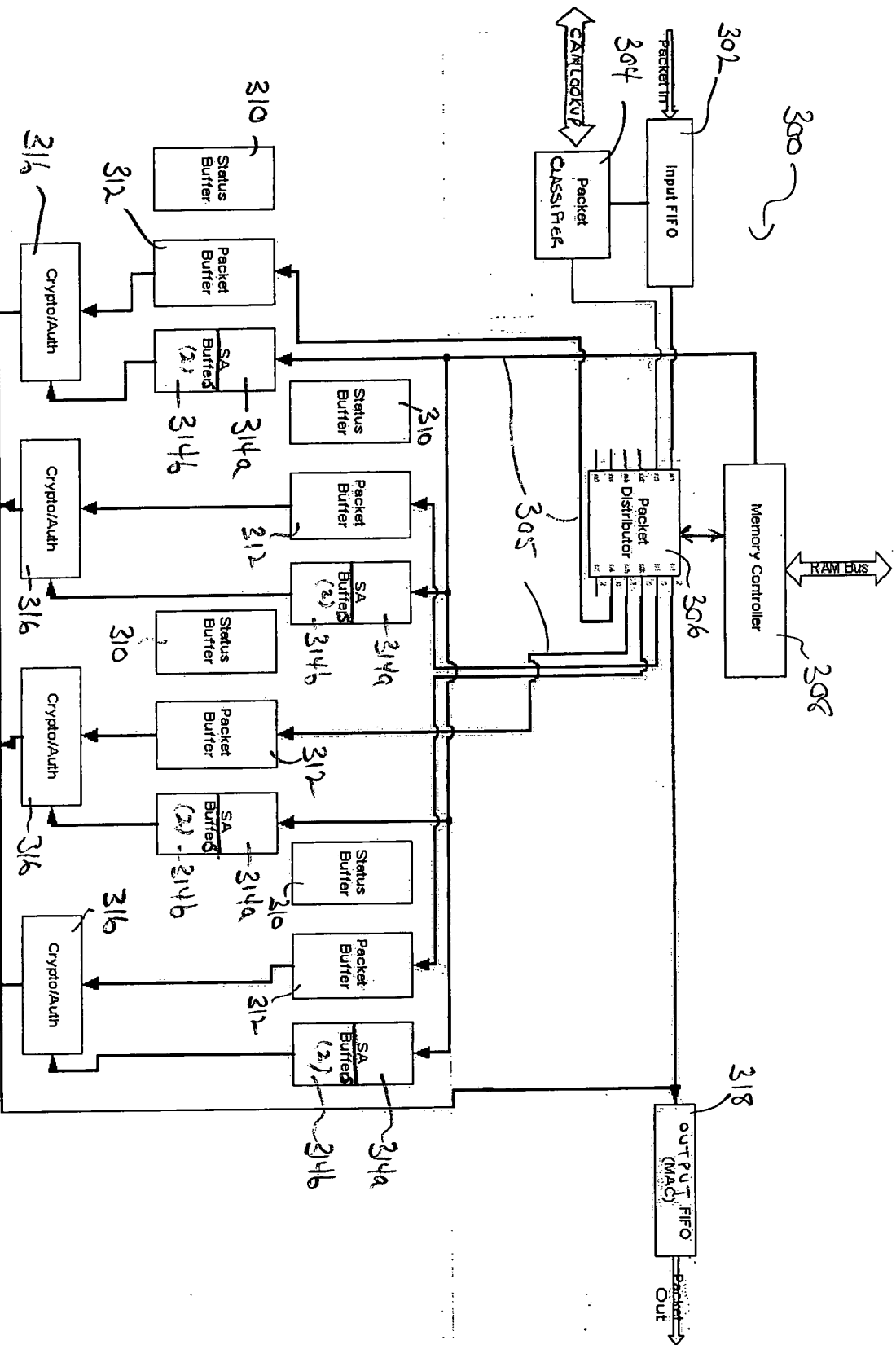


FIG. 3

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The diagram illustrates the packet classification process flow, showing the interaction between memory, packet headers, hash tables, and classification entries.

- MEMORY:** A vertical line representing memory access.
  - PKT HDR ACCESS:** Accesses the packet header, which contains **NEXT PKT DMA ADDR**.
  - HASH TABLE ACCESS:** Accesses the hash table, which contains indices **INDEX 0**, **INDEX 1**, **INDEX 2**, and **REHASH**.
  - CLASSIFICATION ENTRY ACCESS:** Accesses the classification entry table.
- BASE IP HDR, SRC/DST PORT, PROTO, SPI:** A block that receives input from the packet header and the hash table.
- HASH:** A block that receives input from the packet header and the hash table.
- =:** A comparison block that receives input from the **HASH** block and the **CLASSIFICATION ENTRY** block.
- MATCH:** The result of the comparison, indicating a successful match.
- CLASSIFICATION ENTRY:** A block that receives input from the hash table and the classification entry access.

FIG. 4

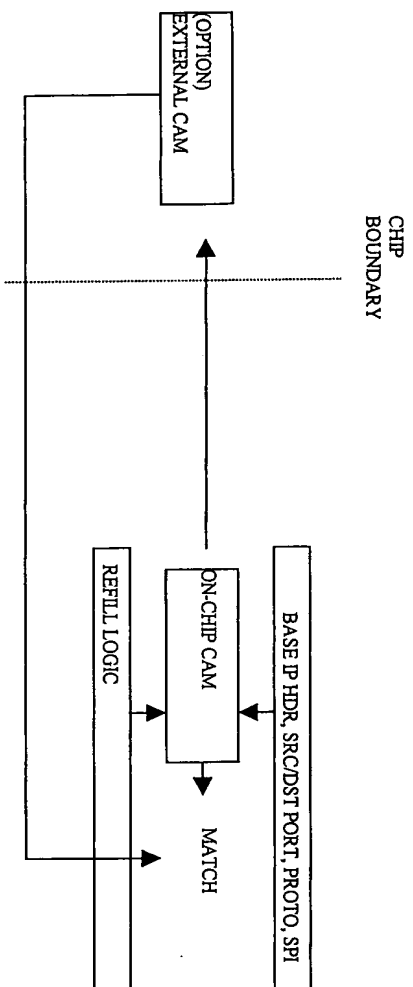


FIG. 5

# REPORT ON THE PROGRESS OF THE WORK

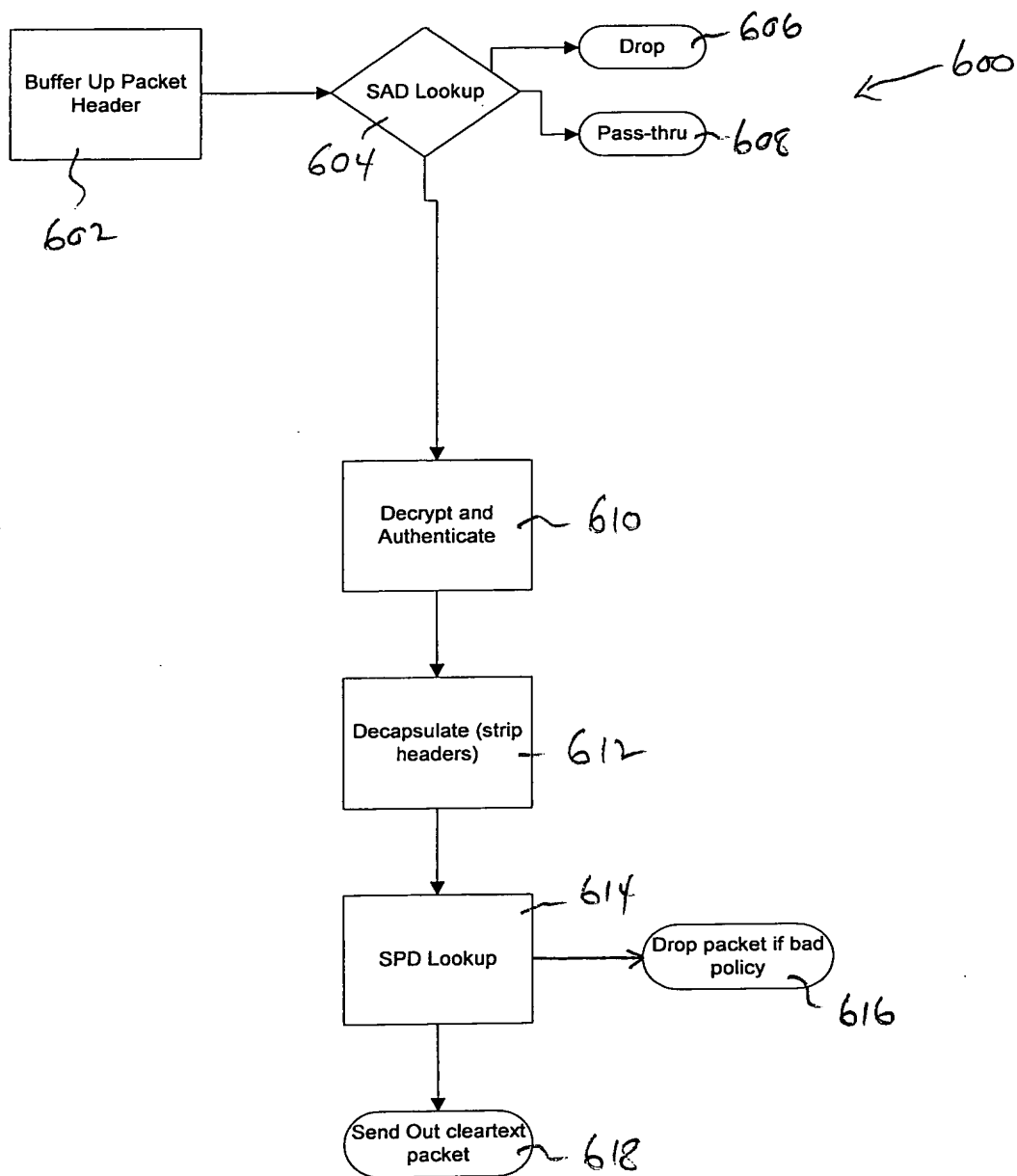


FIG. 6A

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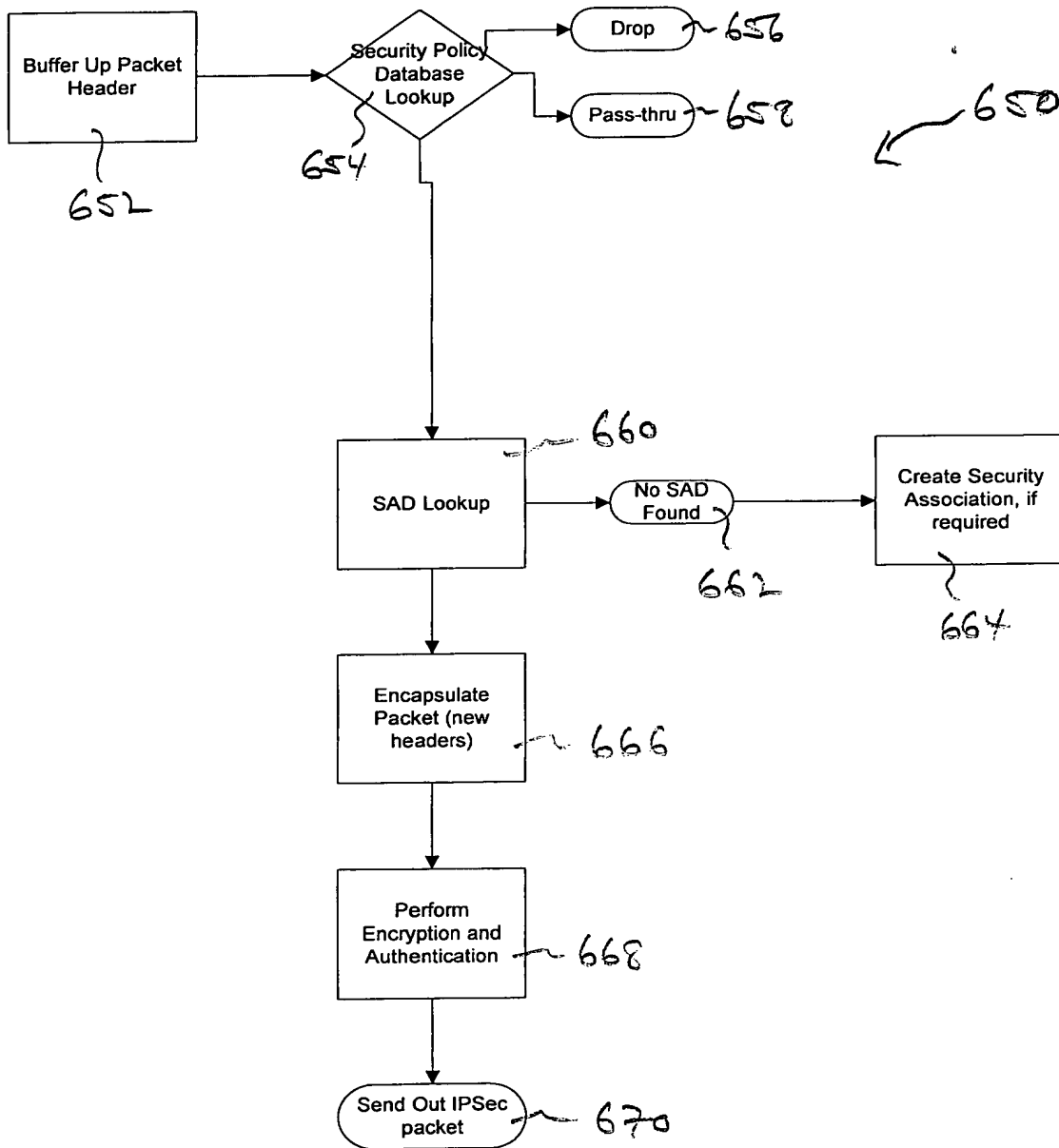


FIG. 6B



The diagram illustrates the high-level architecture of the IPsec Header Stream Processor. It shows the flow of data from input buffers through various processing and caching stages to the final header processing and output.

- TO MEMORY CTRLR**: A dashed line on the left side of the diagram.
- RANDOM NUMBER GENERATOR**: A block at the top center.
- QUAD REQUEST REFILL ENGINE**: A block below the random number generator, receiving input from **WB STATS** and the **TO MEMORY CTRLR**.
- SATC-CL CACHE** and **SATC-AUX CACHE**: Two cache blocks that receive input from the **QUAD REQUEST REFILL ENGINE**.
- HASH**: Two hash blocks, one for the **SATC-CL CACHE** and one for the **SATC-AUX CACHE**.
- ENTRY #0** to **ENTRY #255**: Two large blocks representing the cache entries, each containing a list of entries (ENTRY #0, ENTRY #1, ..., ENTRY #255).
- QUAD HEADER BUFFER**: A stack of buffers on the left, providing input to the **HASH** block and the **IPsec HEADER & TRAILER PROCESSING** block.
- HEADER STREAM BUFFER**: A buffer block that receives input from the **QUAD HEADER BUFFER** and provides input to the **IPsec HEADER & TRAILER PROCESSING** block.
- MATCHING SAdB / AUX DATA ENTRY**: A block that receives input from the **SATC-CL CACHE** and **SATC-AUX CACHE** and provides output to the **IPsec HEADER & TRAILER PROCESSING** block.
- UPDT STATS**: A block that receives input from the **MATCHING SAdB / AUX DATA ENTRY** and provides output to the **QUAD REQUEST REFILL ENGINE**.
- ESP/AH/NONE TUNNEL/ADJ**: A block that receives input from the **MATCHING SAdB / AUX DATA ENTRY** and provides output to the **IPsec HEADER & TRAILER PROCESSING** block.
- CHECK/UPDT SEQ. NO.**: A block that receives input from the **MATCHING SAdB / AUX DATA ENTRY** and provides output to the **IPsec HEADER & TRAILER PROCESSING** block.
- TO & FROM CRYPTO ENGINES**: A block that receives input from the **IPsec HEADER & TRAILER PROCESSING** block and provides output to the **QUAD REQUEST REFILL ENGINE**.
- NEW HDR**: The final output of the **IPsec HEADER & TRAILER PROCESSING** block.

FIG. 7